CLAIMS

1. A feed forward circuit for reducing delay through an input buffer, comprising:

an inverter having an input and an output;

an inverting circuit having an input and an output, the input of the inverting circuit being coupled to the output of the inverter; and

a feed forward transistor having a gate coupled to the input of the inverter, and a terminal coupled to the output of the inverting circuit, wherein the feed forward transistor decreases an amount of time required for the output of the inverting circuit to change state.

2. A feed forward circuit as recited in claim 1, wherein the decrease in the amount of time required for the output of the inverting circuit to change state is at least one gate delay of the inverting circuit.

3. A feed forward circuit as recited in claim 1, wherein the feed forward transistor increases a voltage at the output of the inverting circuit when the input to the inverter transitions to a HIGH state.

4. A feed forward circuit as recited in claim 1, wherein the feed forward transistor ceases to increase the voltage at the output of the inverting circuit when the input to the inverter transitions to a LOW state.

5. A feed forward circuit as recited in claim 1, wherein the inverting circuit includes a p-channel transistor and an n-channel transistor, the p-channel transistor having a first terminal coupled to a core voltage, a gate coupled to the input of the inverting circuit, and a second terminal coupled to a first terminal of the n-channel transistor, the n-channel transistor having a gate coupled to the input of the inverting circuit.

6. A feed forward circuit as recited in claim 5, further comprising a high impedance transistor coupled to a second terminal of the n-channel transistor of the inverting circuit, the high impedance transistor having a terminal coupled to ground.

7. A feed forward circuit as recited in claim 6, further comprising a low impedance transistor coupled to the second terminal of the n-channel transistor of the inverting circuit, the low impedance transistor having a terminal coupled to ground, wherein the low impedance transistor is ON when the output of the inverting circuit is HIGH.

8. A feed forward circuit as recited in claim 7, wherein the low impedance transistor is OFF when the output of the inverting circuit is LOW.

9. A feed forward circuit as recited in claim 1, wherein the feed forward transistor turns off, allowing the voltage at the output of the inverting circuit to transition to a LOW state when the input to the inverter transitions to a LOW state.

10. A feed forward circuit as recited in claim 1, wherein the inverting circuit includes an n-channel transistor and a p-channel transistor, the n-channel transistor having a first terminal coupled to ground, a gate coupled to the input of the inverting circuit, and a second terminal coupled to a first terminal of the p-channel transistor, the p-channel transistor having a gate coupled to the input of the inverting circuit.

11. A feed forward circuit as recited in claim 10, further comprising a high drive pull up transistor coupled to a second terminal of the p-channel transistor of the inverting circuit, the high drive pull up transistor having a terminal coupled to a core voltage, wherein the high drive pull up transistor is ON when the output of the inverting circuit is LOW.

12. A method for reducing delay through an input buffer, comprising the operations of:

sensing a voltage transition change before a voltage at an input to an inverting circuit changes state; and

changing a voltage at the output of the inverting circuit in response to sensing the voltage transition change, wherein an amount of time required for the output of the inverting circuit to change state is decreased.

13. A method for reducing delay through an input buffer as recited in claim 12, wherein the amount of time required for the output of the inverting circuit to change state is decreased by a predetermined first time interval.

14. A method as recited in claim 12, further comprising the operations of:

increasing a voltage at an output of the inverting circuit in response to sensing the voltage transition change; and

increasing an impedance at a drain of an n-channel transistor in the inverting circuit in response to sensing the voltage transition change.

15. A method as recited in claim 14, wherein the voltage transition change is sensed at an input of an inverter, the inverter having an output coupled to the input of the inverting circuit.

16. A method as recited in claim 15, wherein the voltage transition change is sensed using an n-channel feed forward transistor having a gate coupled to the input of the inverter, the n-channel feed forward transistor further having a terminal coupled to the output of the inverting circuit.

17. A method as recited in claim 16, further comprising the operation of decreasing a voltage at an output of the inverting circuit in response to sensing the voltage transition change.

18. A method as recited in claim 17, wherein the voltage transition change is sensed at an input of an inverter, the inverter having an output coupled to the input of the inverting circuit.

19. A method as recited in claim 18, wherein the voltage transition change is sensed using a p-channel feed forward transistor having a gate coupled to the input of the inverter, the p-channel feed forward transistor further having a terminal coupled to the output of the inverting circuit.

20. A voltage transition circuit, comprising:

an inverting circuit for transitioning a first voltage to a second voltage, the second voltage being lower than the first voltage;

a circuit coupled to an output of the inverting circuit, the circuit initiating a voltage transition from a third voltage to the second voltage, the third voltage being lower than the second voltage before the inverting circuit initiates the voltage transition from the third voltage to the second voltage.

21. A voltage transition circuit as recited in claim 20, wherein an input to the inverting circuit is coupled to the circuit so as to control the initiating of the voltage transition from the third voltage to the second voltage.

22. A voltage transition circuit as recited in claim 20, wherein the circuit includes an N-type transistor.

23. A voltage transition circuit as recited in claim 22, wherein a first terminal of the N-type transistor is coupled to the output of the inverting circuit and a second terminal of the N-type transistor is coupled to the second voltage.

24. A voltage transition circuit as recited in claim 22, wherein a gate of the N-type transistor is coupled to the input to the inverting circuit.

25. A circuit, comprising:

an inverting circuit for translating a first predetermined voltage to a second predetermined voltage, the second predetermined voltage being lower than the first predetermined voltage;

a feed forward circuit coupled to an output of the inverting circuit, the feed forward circuit initiating a voltage transition from a third predetermined voltage to the second predetermined voltage, the third predetermined voltage being lower than the second predetermined voltage before the inverting circuit initiates the voltage transition from the third predetermined voltage to the second predetermined voltage.